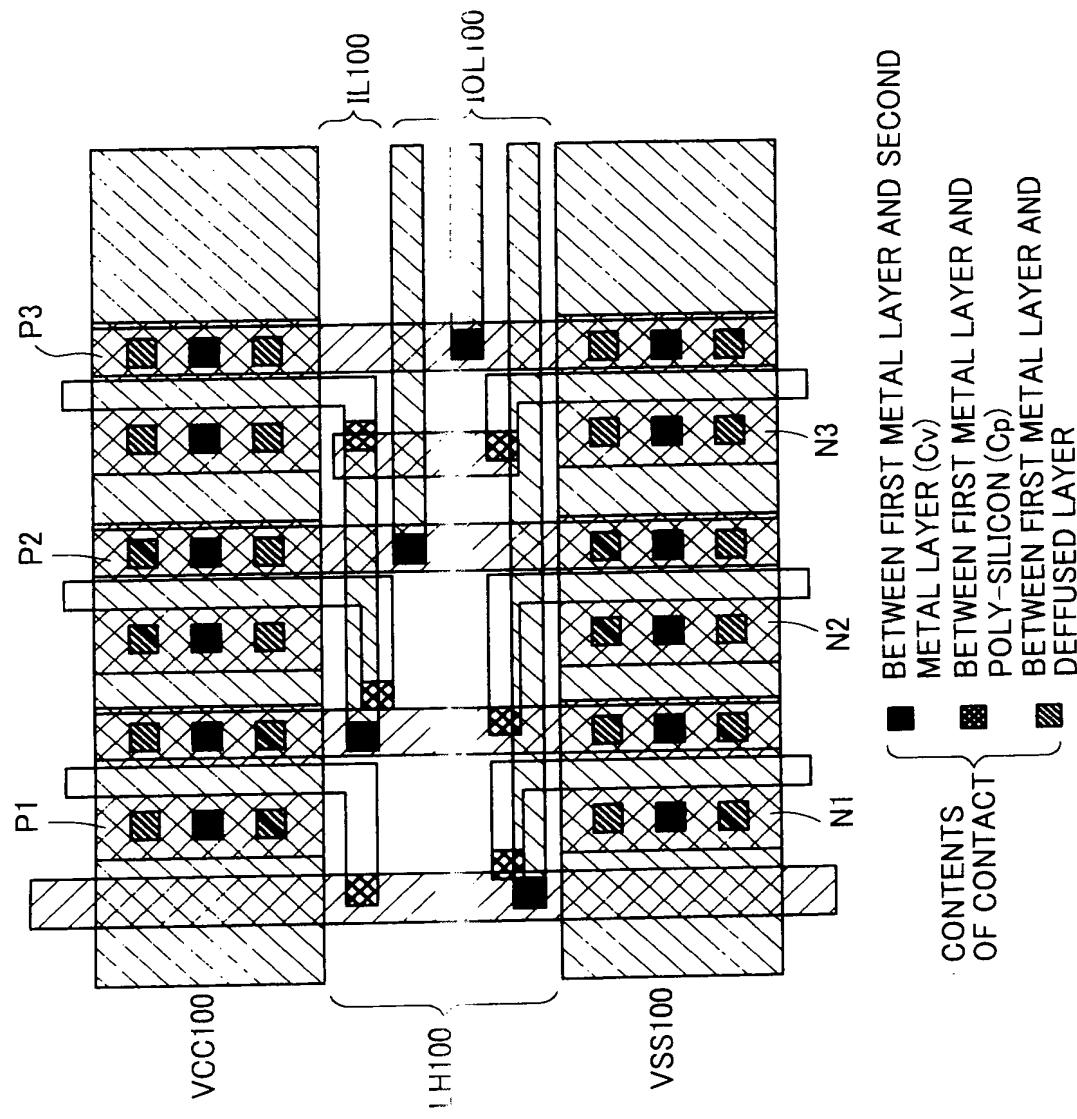


PRIOR ART

FIG.21

LAYOUT DIAGRAM IN CASE PROCESS A DIRECTED TO
FIG.20 IS APPLIED

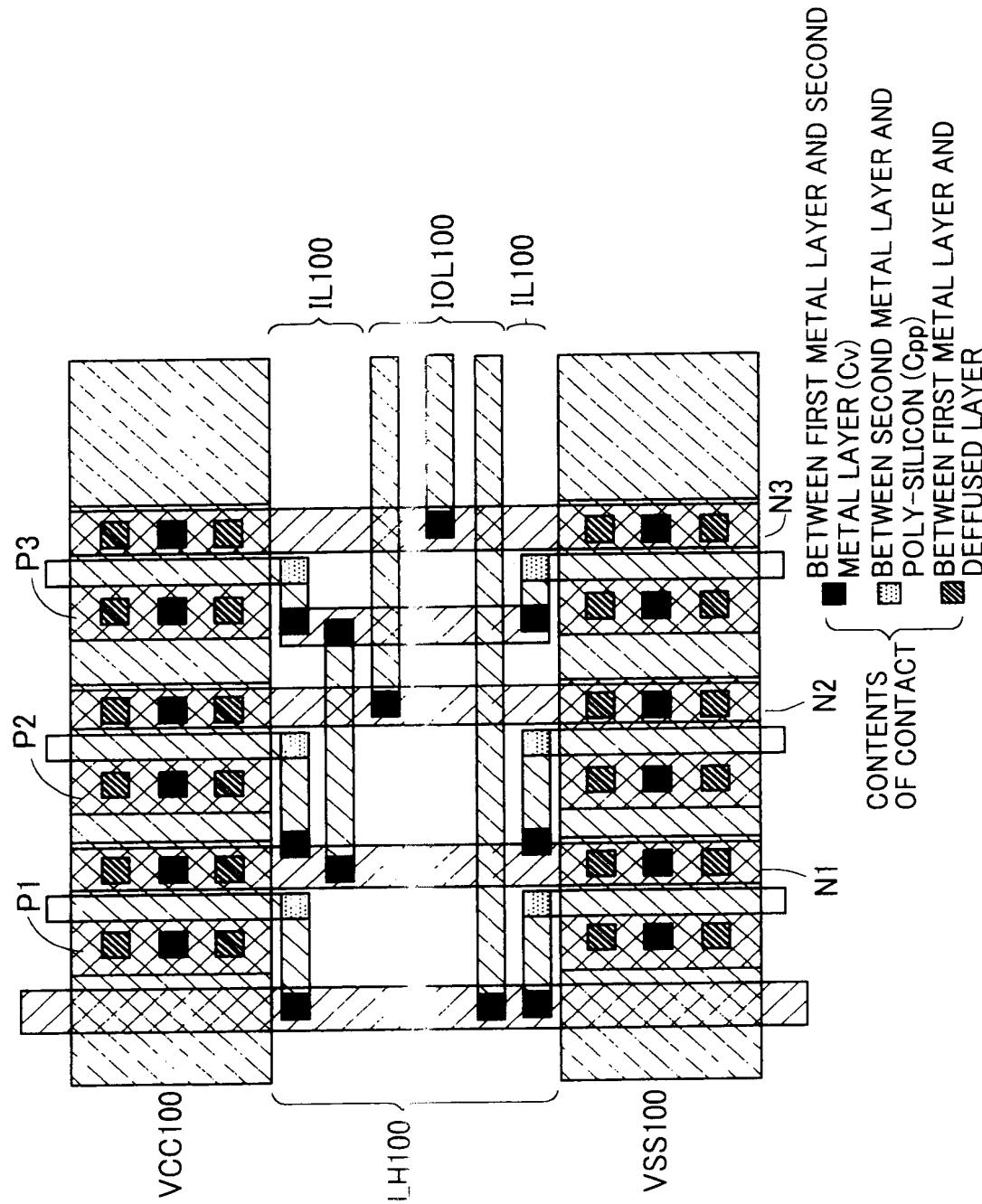


Q.I.P.E. U.S. PATENT & TRADEMARK OFFICE
JUL 21 2003
Title: Semiconductor Integrated Circuit Device W
Enhanced Layout
Inventor: T. Kitahara
Application No. 10-040,460
Docket No. 024016-00022

PRIOR ART

FIG.22

LAYOUT DIAGRAM IN CASE PROCESS B DIRECTED TO FIG.20 IS APPLIED



O-I-P-E
JUL 21 2003
PATENT & TRADEMARK OFFICE
Title: Semiconductor Integrated Circuit Device With Enhanced Layout
Inventor: T. Kitahara
Application No. 10/040,460
Docket No. 024016-00022